White Paper

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A Guide to Making RF Measurements for Signal Integrity Applications

Introduction

Designing a system for Signal Integrity requires a great deal of knowledge and tremendous effort from all disciplines involved. Higher data rates and more complex modulation schemes are requiring digital engineers to take into account the analog and RF performance of the channels to a much greater degree than in the past. Moreover, increasing performance demands are requiring digital engineers move from oscilloscopes and TDRs to vector network analyzers (VNAs), with which they may be less familiar.

Correspondingly, RF measurement groups within companies are being called on by their digital colleagues to help them with making VNA measurements. This paper is intended to review signal integrity-based VNA measurements for digital engineers and correlate VNA measurements to key signal integrity parameters for RF engineers.

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The Driving Need for RF Measurements

Digital Signal Integrity (SI) can be described as a set of measures of the quality of an electrical signal, basically the study of how a pulse distorts during its travels. With the advent of today's Gigabit data rates, the digital community has been forced to solve the types of analog problems that RF/microwave (MW) engineers live with on a daily basis. Therefore, measurements such as standing wave ratio (SWR), insertion loss, leakage between printed circuit board (PCB) traces and delay times, have become parameters that now must be evaluated by digital designers to assure "pulse fidelity." Testing is further complicated by the fact that differential lines and circuits are used to reduce interference. The difficulty increases when many complex circuits are compressed onto a multilayer PC board. On top of that, it is a challenge to contact the desired point on the circuit, since it may be accessed only by using destructive procedures. Test connectors located at strategic points in the circuit offer one solution. Unfortunately, they not only occupy valuable real estate, they may also introduce their own set of problems.

Today, there are increasing problems with reduced transmission quality resulting from adjacent signal effects in multilane PCBs. In addition, high density designs are experiencing increased skew due to differences in lane wiring lengths. In high-speed signal transmission, frequency and data-pattern dependencies cause worries about reduced waveform quality. As a result, it is no longer sufficient to perform evaluations by measuring the bit-error-rate (BER), jitter and waveform quality of each lane independently. Today's high-speed, multi-lane serial communications standards require total evaluation of multi-lanes using multichannel test solutions to perform quantitative measurements – as well as RF/MW instrumentation with sufficient performance to make these measurements.

New technologies continue to enter the market as high speed serial data rates advance from 15 Gb/s to beyond 50 Gb/s (Figure 1) per channel for 40 Gb/s to 400 Gb/s systems. Conventional logic-emulating non-return-to-zero (NRZ) signaling is being replaced by PAM4, a 4-level pulse amplitude modulation scheme that takes half the bandwidth to transmit the same payload as the equivalent NRZ signal. PAM4 challenges signal integrity, test, and design engineers responsible for SerDes (serializer/deserializer) components, interconnects, backplanes, cables, connectors, circuits, and complete systems. The problems solved by PAM4 outweigh the problems it introduces, but PAM4's increased complexity means that we must address a host of new issues.

Figure 1. Advances in high speed design, such as 100G+ applications are driving the need for improved accuracy in signal integrity applications. (Images courtesy of Finisar)

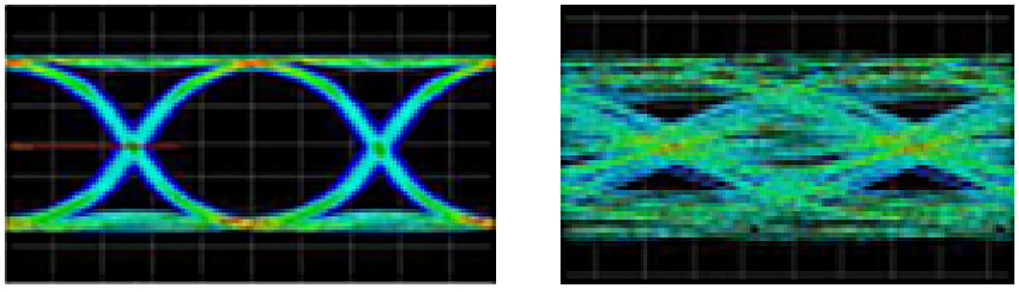
Understanding Signal Integrity Terms and Measurements

Eye Diagrams

An eye diagram is the result of superimposing the 1's, 0's and corresponding transitions of a high speed digital signal onto a single amplitude, versus time display. The resulting waveform resembles an eye, hence the name eye diagram. The time axis can be normalized for 2 bits for easy viewing, with the 1-bit "eye opening" in the center of the display and one-half bit on both left and right of the center eye (for viewing transitions). Transitions in the digital signal that infringe on the center of the eye can eventually cause errors or eye closures

In general, the more open the eye, the lower the likelihood that the receiver in a transmission system may mistake a logical 1 bit for a logical 0 bit, or vice versa. The bits that have errors compared to the overall bits is called BER, generally the lower the BER the better. BER can also stand for Bit Error Rate, which is the number of bit errors per unit time. It's important to note that the eye diagram does not show protocol or logic problems. Using this eye diagram, we can easily view signal impairments in the physical layer – in terms of amplitude and time distortion (Figure 2).

Both the Anritsu VectorStar and Shockline VNAs offer the ability to generate eye diagrams. VectorStar provides real time capability to allow test engineers to make circuit adjustments and quickly see the results. Shockline VNAs are able to generate eye diagrams in a post processing mode, allowing for quick checking of performance even on the manufacturing line.



(a) Good eye pattern *(b) Degraded eye pattern*

Figure 2. Eye diagrams show amplitude and time distortions which allow signal impairments in the physical layer to be easily seen.

Dispersion

An ideal rectangular waveform is formed by adding odd multiples of a sine wave at the data rate. (To be exact, it is formed by summing 1/N of the amplitude of N multiples of the harmonic.)

$$f(x) = \frac{\pi}{4}\left(\sin(x) + \frac{1}{3}\sin(3x) + \frac{1}{5}\sin(5x) + \frac{1}{7}\sin(7x) + \cdots\right)$$

When the N multiples of the frequency components are superimposed, the sine wave gradually changes to a rectangular waveform. The high frequency components determine rise time, the time over which a 0 becomes 1; the time over which a 1 becomes 0 is the fall time. Lower frequencies make up the "flat top." The transition becomes sharper, as seen by the green arrows in Figure 3, as more components are added.

As the signal above passes through a micro-strip line, all of the spectral lines do not propagate at the same rate. This is called dispersion. Since the individual spectral lines do not propagate at the same rate, they do not arrive at the termination at the same time. This causes pulse distortion.

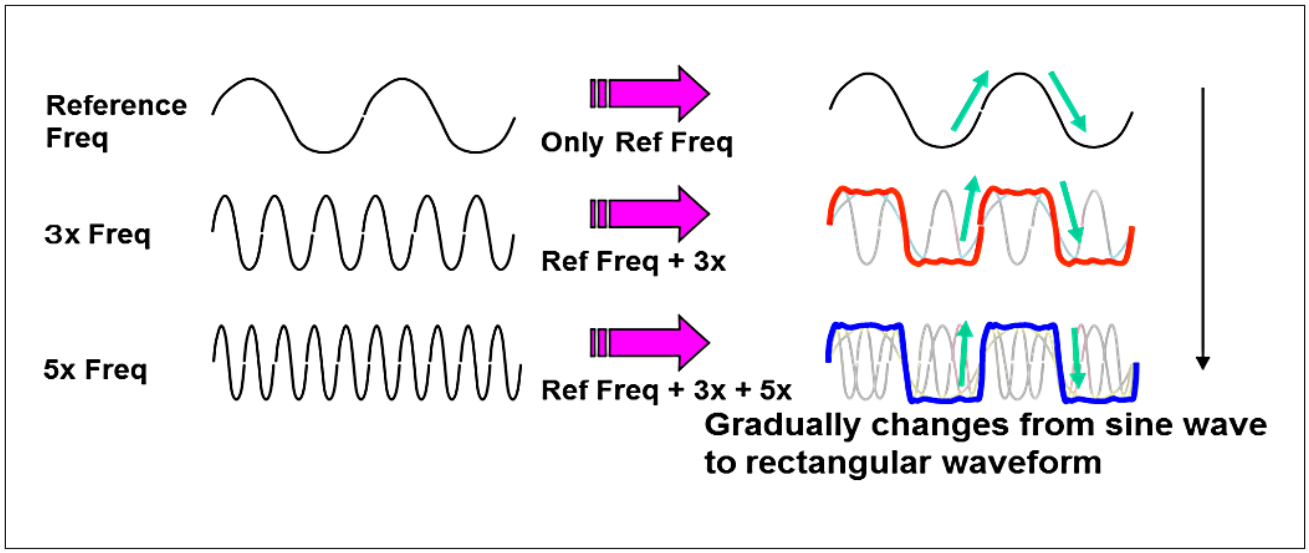


Figure 3. A square wave is composed of an infinite number of odd harmonics.

High Frequency Loss /Attenuation

Typically, PC boards have very high loss the higher you go in frequency (Figure 4), and this high-frequency loss tends to close the eye. At the Gigabit rates in use today, PC board traces can have appreciable copper loss, skin effect (loss due to the microwave portion of the signal traveling only on the surface of the trace), as well as dielectric loss (absorption of energy due to substrate material). These are all frequency dependent losses. Loss can reduce the level to the point where a “one” is below the logic threshold. Longer paths and higher frequencies lead to predictably greater losses.

Now, there are a number of things that you can do to mitigate those losses. Number one, you can use lower-loss materials, which may or may not be practical, because lower-loss materials are typically more expensive. You can use shorter path lengths to minimize that high- frequency loss, and that may or may not be practical, due to where the components are placed on the PC board.

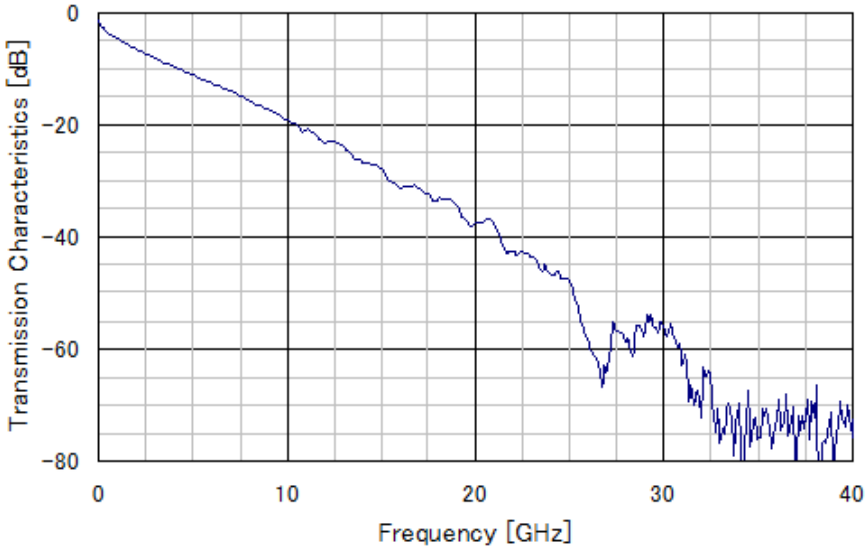


Figure 4. Attenuation or loss increases with frequency and may negatively impact the eye opening.

Emphasis

You can use an eye opener, which is basically a filter that helps open the eye by adding emphasis to specific portions of the signal– essentially attenuating some of the lower frequency losses and equalizing some of the higher frequency losses. Emphasis adds high frequency energy to the transmit waveform by accentuating the rise/fall times which is where all of the high frequency content resides. This increased high frequency content in the data helps to offset the high frequency losses in the channel.

The challenge is that it is difficult to find the ideal settings from the many possibilities. One method is to search for the ideal settings while verifying the output waveform, but this method takes an extremely long time and it is hard to come up with an explanation of why those settings are ideal. The goal is to find a rational method of determining the ideal emphasis settings from many complex possibilities so that we could simplify and shorten the emphasis setting procedure, helping to cut measurement and design verification times.

An easier way is to use a VNA to measure the S-parameters of the transmission path. Then you generate an .s2p or an .s4p output file on the VNA and import it into the BERT (Bit Error Rate Tester). Based upon those transmission path S-parameters, many BERTS can determine the tap weights, giving you the ideal emphasis setting for that particular transmission path. See Figure 5.

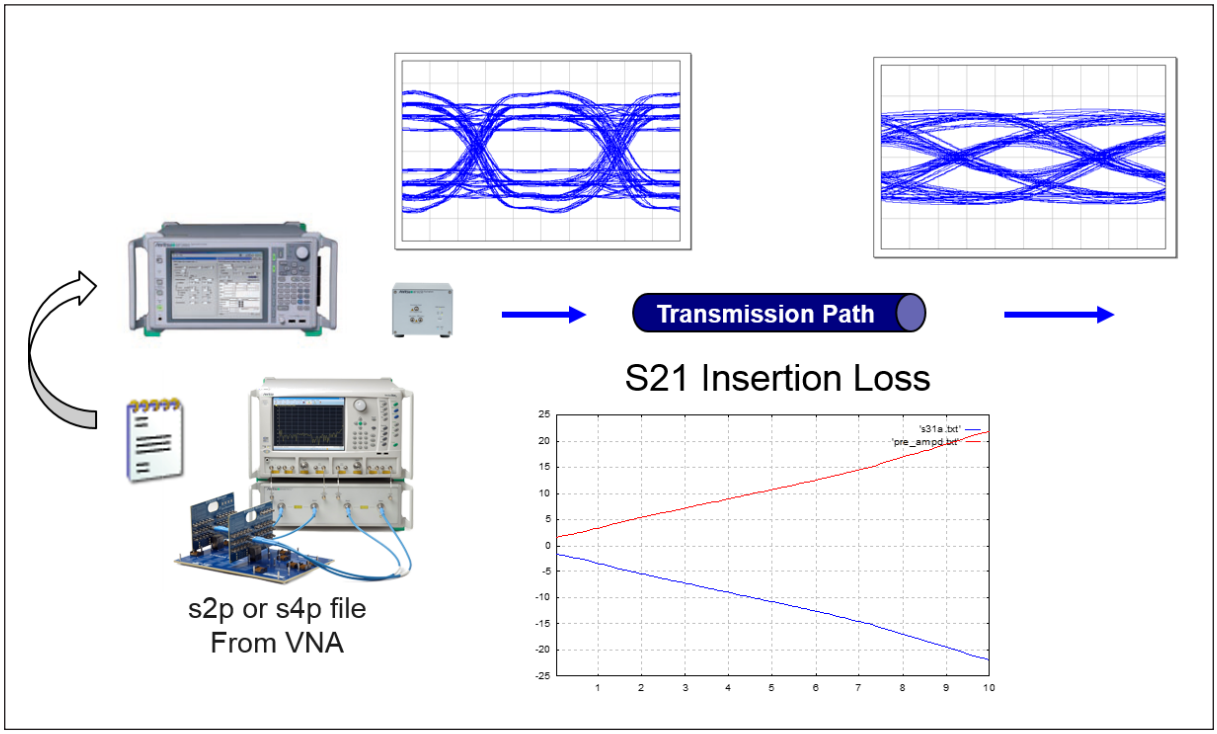


Figure 5. Test setup block diagram for determining the ideal emphasis setting for a given transmission line [Blue trace s31a.txt is the measured insertion loss, Red trace pre_ampd.txt is the corresponding emphasis].

Inter-Symbol Interference (ISI)

One of the other causes of eye closure in high-speed systems is Inter-Symbol Interference or ISI. ISI can be caused by a number of factors, such as mismatch issues (often a dominant cause) and dispersion. Because low frequency components travel faster than high frequency components (dispersion), there is a “bunching” of the data stream and it results in eye closure. BERT measurements are very good at identifying that there is an ISI problem, but not why (Figure 6).

VNAs are very good at characterizing dispersion in a channel by measuring group delay. In a group delay versus frequency plot, you can see that the low-frequency component transit time is shorter than the high-frequency components (Figure 6). The non-constant group delay over frequency is what may be causing the ISI.

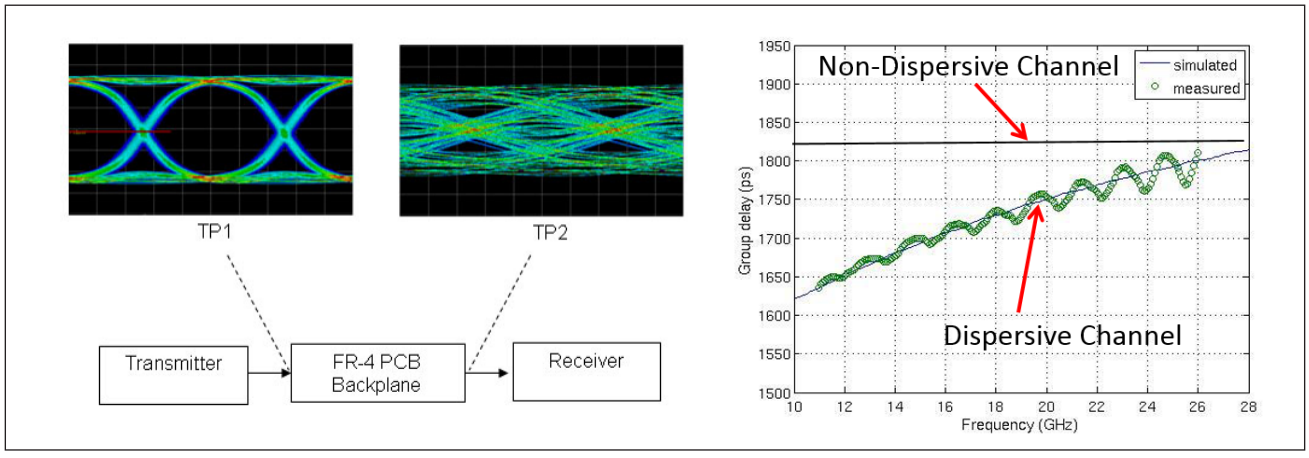


Figure 6. BERTs are very good at finding ISI problems. VNAs can help determine the cause of the problem.

Crosstalk

Crosstalk is an undesired coupling that occurs as a consequence of micro-strip traces or unshielded dual conductor cables in close proximity to each other. This is due to capacitive coupling and inductive coupling along the lines. Maintaining several line widths of physical separation on the board is ideal, but difficult to implement, since space is always at a premium. Printing grounded areas between the traces or adding ground vias provide a measure of decoupling of the "E" fields, but also requires additional board space. Other mitigation options include grounding strategies, barrier walls, tapers and other layout items. Parasitic coupling can occur anywhere along a line; however, the end terminations are especially problematic. The corresponding crosstalk is referred to as Near End CrossTalk (NEXT) and Far End CrossTalk (FEXT). NEXT and FEXT are in respect to the port to which the stimulus is applied. In actuality, crosstalk can occur anywhere along a line, whether it is dual conductor or single-ended. For example, Figure 7 shows a dual conductor line with the required connections to measure NEXT and FEXT.

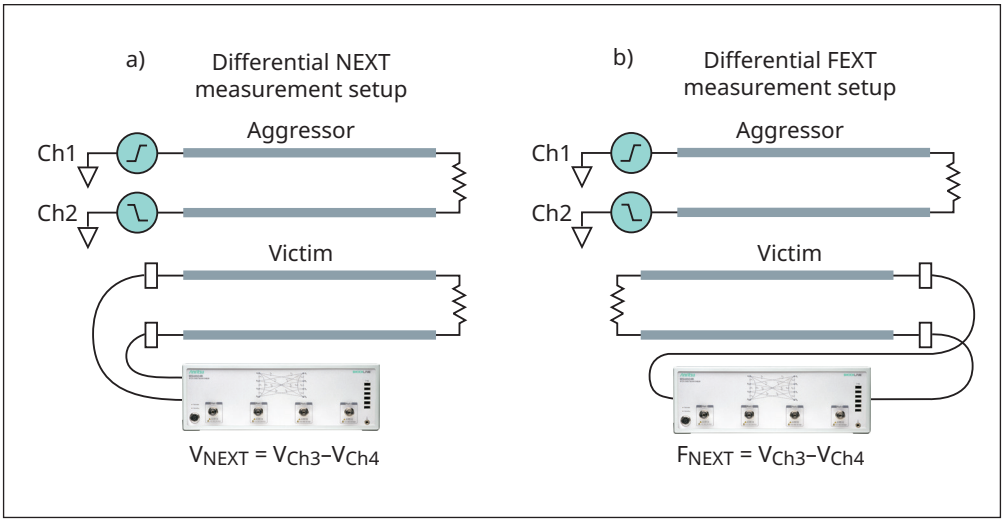


Figure 7. Closely spaced parallel micro-strip lines can couple signals unintentionally.

Crosstalk is generally specified as a percentage of the signal that appears on the relative victim line, relative to the aggressor line. It can also be expressed in terms of dB below the driven line level. When using a VNA to perform this measurement, the frequency span should be the same as the intended use for the path under test – so leakage levels will be accurate.

When performing crosstalk measurements, the ends of the trace or cable not being tested must be terminated in the characteristic impedance of the line (nominally 100 Ohms in a dual conductor configuration). NEXT and FEXT can be measured simultaneously. In this configuration, NIST (National Institute of Standards and Technology) traceable 50 Ohms (to ground) calibration components can be used to calibrate the VNA. Figure 8 shows NEXT and FEXT measurements of a standard CAT 5 cable with RJ45 connectors. When measuring FEXT, the analyzer's signal must travel the length of the cable and then return back to the analyzer. Since the analyzer measures roundtrip time, in this mode the measured time is divided by two (when calculating the distance to the origin of the crosstalk).

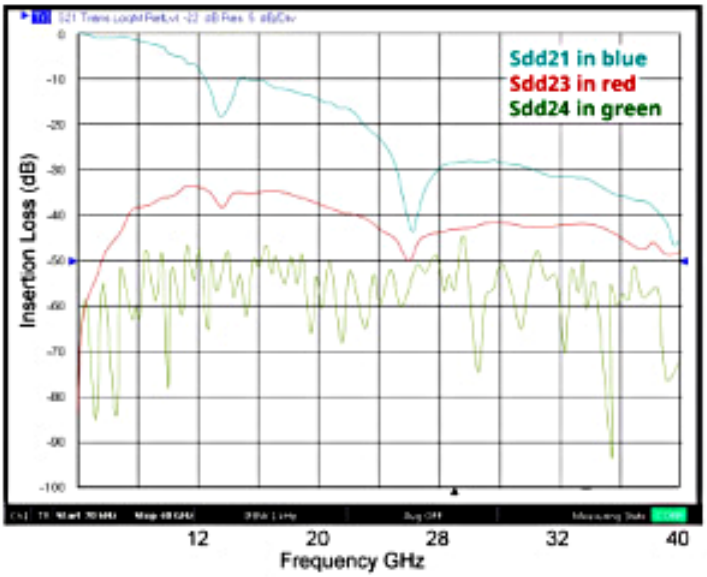


Figure 8. Insertion loss, NEXT and FEXT for a differential channel in a two channel differential system. S_{dd21} (insertion loss), S_{dd24} (NEXT), and S_{dd23} (FEXT).

Balanced or Differential Mode

Balanced or differential lines provide rejection of external fields and have minimal radiation (Figure 9). Balanced signaling is two conductors (with an optional shield) that have equal impedance to ground. Differential signaling is two conductors (with an optional shield) transmitting the same signal at opposite polarity. If the transmitted signal is the same polarity, then the circuit is operating in common mode. If a device has both dual conductors operating in differential or common mode and a single ended conductor, then it is said to be operating in mixed mode.

Slight imperfections in the lines due to manufacturing tolerances and nearby metallic objects distort the fields, so the common mode signal is never zero. The degree to which cancellation is accomplished is known as the Common Mode Rejection Ratio (CMRR), often measured as the differential response to a common-mode input. Despite these imperfections, differential lines are commonly used to interconnect devices, boards and layers. An added benefit of using differential geometry is that ground planes are not required to maintain characteristic impedances, which would be the case if single-ended micro-strip geometry was employed.

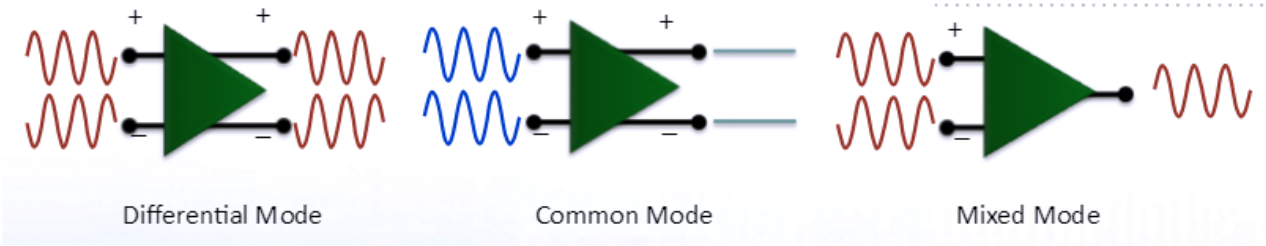


Figure 9. Differential lines provide rejection of external fields, have minimal radiation and are commonly used to interconnect devices.

Whenever there is imbalance in a differential system, the fields no longer completely cancel, which causes them to radiate in proportion to the imbalance. Similarly, external fields can induce currents in a differential pair that are not equal in amplitude and opposite in phase, so they no longer cancel. The resultant current is called common mode current, which produces crosstalk.

On multilayer PC boards, “vias” are used to pass the signal from one layer to another. While they are designed to make a seamless transition, they do not. Therefore, a portion of the signal is reflected back to the source forming a standing-wave. In a differential system, if the two reflections are not identical, mode conversion is introduced. Differential end connections are another area where standing waves are a problem and where mode conversion may take place. Again, whenever there is imbalance in a differential system, the fields no longer completely cancel, which causes them to radiate in proportion to the imbalance. In single-ended circuits, undesired coupling between traces is also problematic.

Differential VNA measurements can be acquired either with a four-port VNA (two differential pairs) or with a four-port VNA that uses four single-ended measurements and the superposition theorem applied to calculate differential measurements (Figure 10). The theorem provides accurate data, provided the device under test is in its linear region. This will be discussed in more detail in a later section.

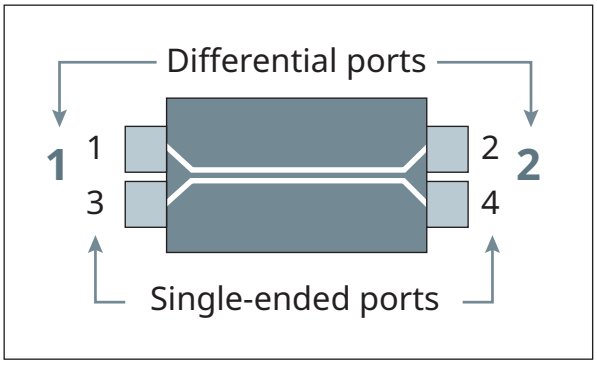


Figure 10. Differential VNA measurements can be acquired either with a four-port VNA (two differential pairs) or with a four-port VNA that uses four single-ended measurements.

Sixteen parameters are required to describe the various combinations of differential and common mode signals, which may be used to characterize a differential path (Figure 11). Single-ended VNA measurements may be taken with the VNA, then calculated to determine differential characteristics.

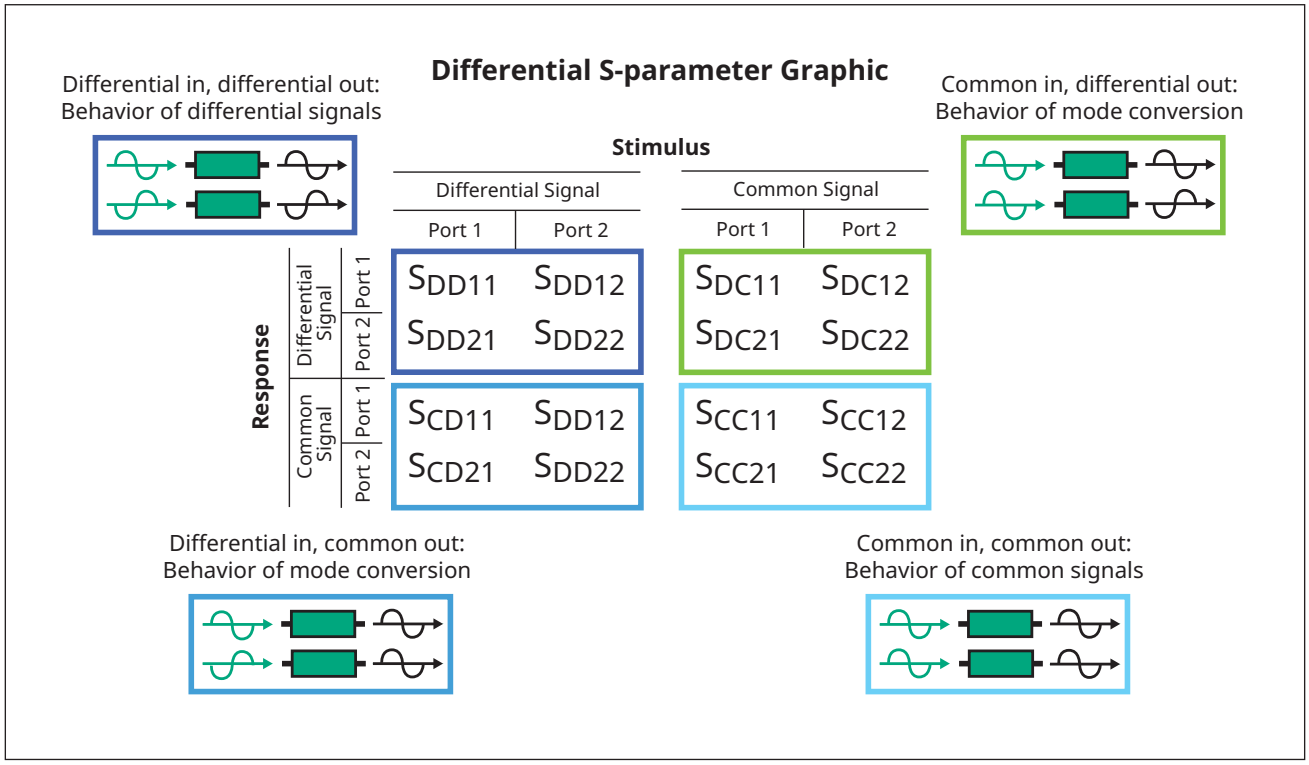


Figure 11. Sixteen parameters are required to describe the various combinations of differential and common mode signals.

Skew

Extremely high data rate signals can be created by combining multiple parallel paths at lower rates. For instance, a 40 Gigabit system can utilize four parallel 10 Gigabit paths. Where this is done, care must be taken to ensure that the propagation time through the various paths is the same. The difference in propagation time is called skew; skew between traces of a single differential pair is intra-pair skew and skew between two or more differential pairs is inter-pair skew. If the connecting medium is coaxial cable, tight control of mechanical length and dielectric tolerances will produce minimal problems with skew. However, when differential twisted pairs are the conducting medium, the number of turns per inch is a critical factor in determining propagation time. Commercial CAT5e/6 cable can have as much as 10 nanoseconds of skew between the paths in a one hundred foot run. This equates to as much as ten feet of electrical length within the same cable!

Skew is a time/electrical length measurement and is easily determined using the time domain capabilities of a VNA. Where both ends of the cable are available (prior to installation), it becomes a straightforward insertion phase measurement. After installation, reflection phase can be used to measure differences in propagation time. For this measurement, the far end is shorted, so a high reflection is presented to the instrument. This makes it easy to derive comparisons of roundtrip time. Roundtrip time must be divided by two, either offline or within the measuring instrument. All Anritsu VNAs can provide the one-way or round trip times in time domain reflection mode.

Jitter / Noise

Noise is present in every electronic device. For example, when the input to a TV is disconnected, audible noise is heard. Noise covers a wide frequency range instantaneously and is referred to as white noise. Well-designed systems have sufficient noise margins, called signal-to-noise ratio. The higher the ratio, the better the system immunity to noise. As a digital signal becomes attenuated and approaches the noise level, the threshold between logic levels becomes unstable. Appreciable noise on the clock will manifest itself as jitter.

Total jitter is a product of both random jitter and deterministic jitter (Figure 12). Random Jitter is unpredictable electronic timing noise or thermal noise. Deterministic jitter is a type of clock timing jitter or data signal jitter that is predictable and reproducible. The peak-to-peak value of this jitter is bounded, and the bounds can easily be observed and predicted.

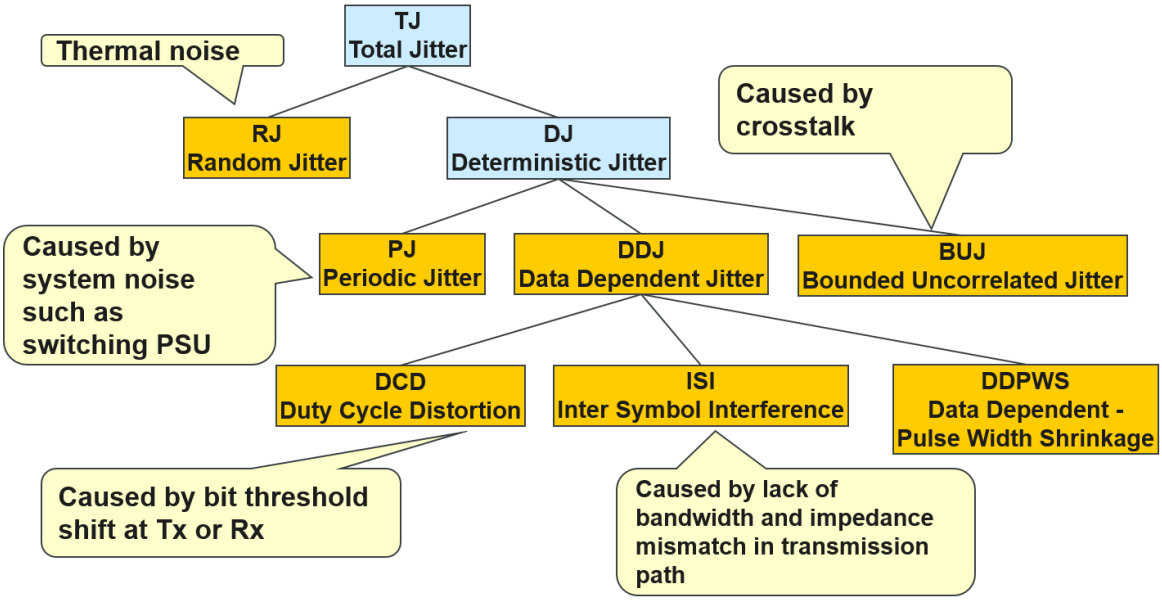


Figure 12. Total jitter is caused by a wide variety of factors.

Jitter testing (also called Timing Jitter) is important to SI engineers, especially as clock frequencies increase in digital electronic circuitry. Higher clock frequencies have commensurately smaller eye openings, and thus impose tighter tolerances on jitter. Major contributors to jitter are: thermal noise, cross talk and “noisy ground connections”. They all cause signal instability at the trigger point from pulse to pulse. Jitter can artificially be injected into the system to test jitter tolerance.

Standing Wave Ratio

Standing Wave Ratio (SWR) was a parameter originally focused in the domain of antenna designers. However, any high frequency generator (i.e., chip output), conducting medium PCB trace or a load (the following chip input), must all be impedance-matched to transfer maximum power. While logic circuits are not dependent on transferring maximum power, when maximum power is not transferred, the portion that is not transferred is reflected back to the source, causing standing waves; SWR is the ratio of the peak amplitude of a standing wave to the minimum amplitude of a standing wave. The result of standing waves on a pulsed signal is ripple on the “flat top.” Ripple can cause false triggers, as seen in Figure 13.

When laying out a circuit, the distance between chip outputs and inputs, as well as their return paths, should be kept as short as possible with reference to wavelength. Each of the frequencies which make up the pulse has its own wavelength (velocity / f). This means that a small percentage of a wavelength at the Bit Rate will be a much higher percentage of a wavelength at the higher order components of the Bit Rate. For instance, a .05 wavelength (velocity / “Bit Rate”) represents a .25 wavelength at the fifth harmonic. Since each spectral line has its own SWR, swept frequency SWR measurements are required across the range of frequencies – which is often five to ten times wider than the data rate. SWR data is in linear terms. Corresponding data in logarithmic terms is Return Loss (dB). Standing waves may be generated when test connectors are added for the purpose of troubleshooting. Prototypes may be built with strategically located test connectors that can be removed in production units.

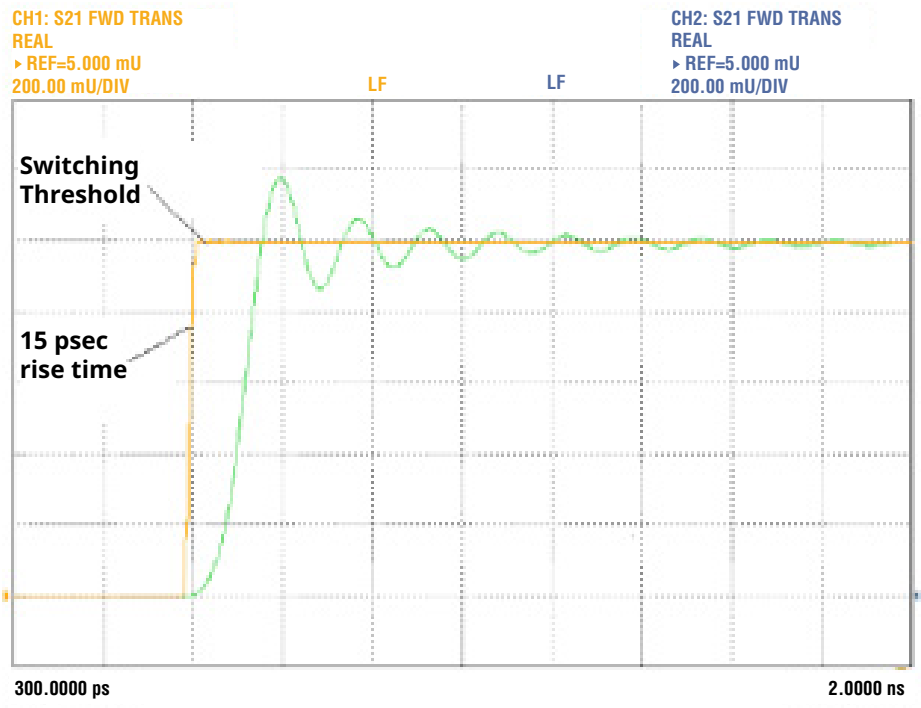


Figure 13. The result of SWR on a pulsed signal is ripple which can cause false triggers.

Channel Operation Margin (COM)

At high data rates, we can't always reasonably expect open eye diagrams at the receiver, so we need sophisticated tools to analyze signal quality. COM (channel operating margin) is a signal-to-noise-like quantity that combines jitter, noise, crosstalk, and ISI plus the effects of equalization into a single figure of merit. It's like the effective SNR at the receiver input.

Measuring COM is an involved process based on S-parameters. The differential S-parameters of the channel, S_{dd21}, are used to calculate the ISI signal impairment and the extent to which it can be removed by equalization. The resulting signal amplitude is given by A_S.

FEXT is calculated from the crosstalk elements of the system S-parameters. Along with crosstalk and the remaining effects of ISI after equalization, the transmitter distortion, random jitter and noise are all combined and used to estimate the vertical eye closure defined with respect to a specified system error rate. COM is the ratio of the signal amplitude, A_{signal} to the vertical eye closure, $A_{NoiseXtalk}$,

By specifying COM, high speed standards permit design flexibility. Most standards require COM > 3 dB. Since COM neglects common mode noise and NEXT and approximates the interaction of equalization and crosstalk, it's not a substitute for a proper model.

$$COM = 20 \log \frac{A_{signal}}{A_{ni}}$$

For more information on COM, see Anritsu' 11410-00989A Measuring Channel Operating Margin white paper.

Why Use BERTs, VNAs, or TDRs

BERTs

Most signal integrity engineers are already using BERTs, oscilloscopes (in a time domain reflectometer {TDR} mode), TDRs, or combination products for their signal integrity applications. These instruments are very useful in measuring the jitter, the bit error rate, and eye openings for that digital hardware. Anritsu offers a series of BERTs scope combination products that provide bit error-rate measurements to 32 Gb/s and with an external MUX/DEMUX they can go up to 64 Gb/s (Figure 14).

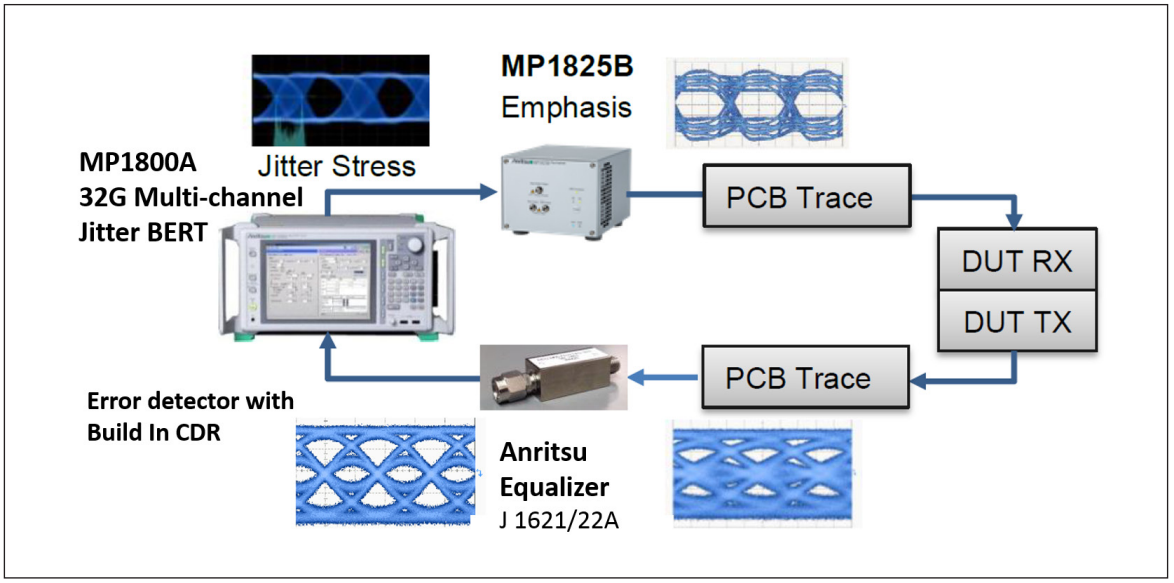


Figure 14. BERTs are excellent at determining if there are any issues with jitter, the bit error rate, and eye openings.

BERTs can handle a wide range of digital encoding schemes: NRZ, PAM-4, PAM-8. They also have a wide range of pseudorandom binary sequence (PRBS) bit streams in both single and dual output pulse pattern generators. They've got the ability to characterize jitter. They can do eye-diagram measurements, and the Anritsu solution is a very reconfigurable mainframe.

The bottom line is that BERTs are excellent at determining whether there are any problems with your device under test. However, they are less helpful at finding the root cause of the problem.

VNAs

Vector Network Analyzers, or VNAs, are very useful in determining the actual cause of a signal integrity issue; see Figure 15. For example, they are excellent tools for understanding what is causing eye closure in high data rate systems. With wide frequency bandwidths, they allow channel characterization that can be a broad as 70 kHz to 145 GHz. This wide bandwidth helps build accurate models (by including multiple harmonics and providing a low end frequency for better DC extrapolation), as well as provide very accurate resolution in the time domain for locating defects in the channel; see Anritsu's whitepaper entitled "Signal Integrity – Frequency Matters."

VNA's are very helpful in understanding the physical structures and their imperfections. For example, for a printed circuit board, no manufacturing process is perfect. VNAs are good for analyzing real world channel defects, like exceeding tolerances on PCB artwork, plating and dielectric thickness variations. They can be used to evaluate connector performance, construction and how well they are mounted. They can be used to analyze multilayer PCB stack ups and find imperfect vias or ground plane issues.

Also, most signal integrity channels use test fixtures during their characterization. VNAs have a very good capability of determining the effects of these fixtures. Network extraction creates a model that is used to minimize the effect of the fixture. De-embedding is the process of applying the model to remove the effects of the fixture on the measured results. Fixture embedding/de-embedding will be discussed in more detail in a later section.

In addition, VNA results can help you correlate your simulations to measured results. Many design engineers are using EDA tools to simulate their channel before they are built. This can speed the time to market for a design. Verifying simulations can provide insight into the expected performance of your design.

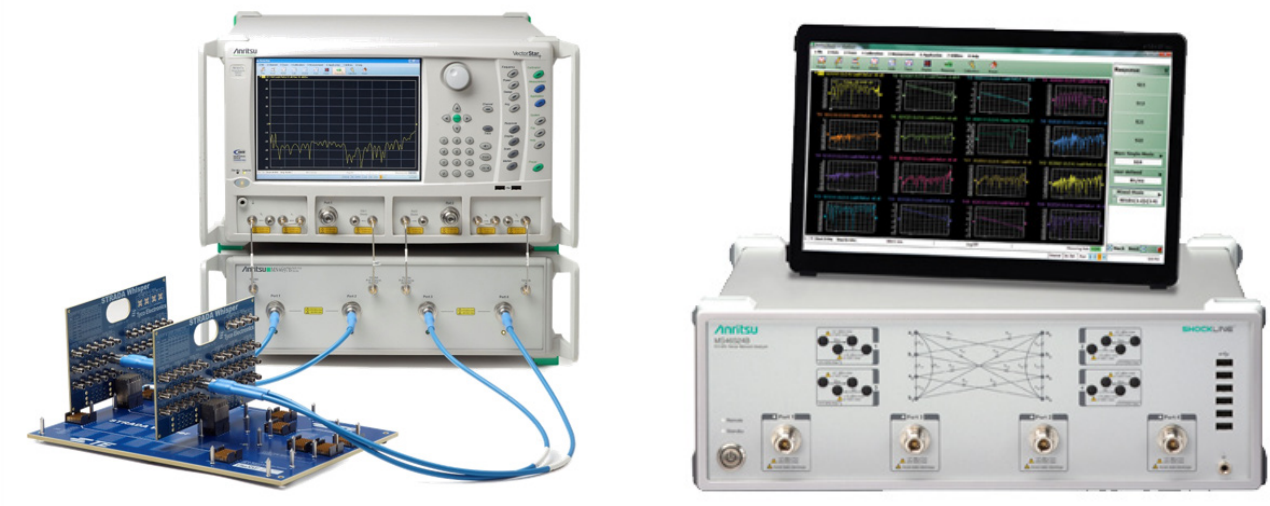


Figure 15. VNAs are useful for determining the cause of a signal integrity issue.

Time Domain Reflectometers (TDR)

In the early days of signal integrity, the Time Domain Reflectometer (TDR) was used to display reflection coefficient / impedance versus distance. The TDR supplied a fast rise time stimulus pulse to the path under test and displayed the amplitude of the return signal versus time.

Since TDRs are broadband measurements and the noise of an instrument is proportional to the instrument bandwidth, they tend to have high noise floors and low dynamic range. The typical dynamic range of a TDR test set is around 40 dB, while the dynamic range of Anritsu's VectorStar and Shockline VNAs are typically above 100 dB—a million times that of a TDR. In addition, with their short rise-time voltage steps and intrinsic time base uncertainty, TDR measurements suffer synchronization problems that can lead to inconsistent S-parameters and make it impossible to model PAM4 problems like timing skew.

While TDR can be used to measure crosstalk S-parameters, at least in principle, their limitations make it difficult for them to assess the weak coupling between victims and aggressors with any accuracy. Without accurate NEXT and FEXT S-parameters, they can't be used to make accurate COM measurements or use their measured results in IBIS-AMI (Input/output Buffer Information Specification – Algorithmic Modeling Interface) models.

In addition, the effective frequency range of a TDR-like measurement is set by the rise time of the pulse. There is obviously a need sometimes to control the frequency range (if the fixture radiates above frequency X or something in the DUT resonates at frequency Y). Historically, this has not been easy to do with instruments used for TDR (TDRs and oscilloscopes). Newer instruments have included some ability to change the rise time, but it is not easy and the choices are not usually continuous. Contrast that to a VNA where one can dial in whatever frequency range wanted (even after calibration assuming interpolation is being used).

Determining Frequency Range

Max Frequency

It will come as no surprise that as bit rates increase, then the upper frequency limit for evaluating backplane and interconnect transmission characteristics must also increase. Higher speeds basically translate into higher test frequencies being required to perform measurements to the 3rd or 5th harmonic of the NRZ clock frequency. For example, for a 28 Gbps data rate this means either 42 GHz or 70 GHz stop frequency for an S-parameter sweep. Figure 16 shows a spectrum of a 14 GHz square wave which would be the clock frequency for a 28 Gb/s NRZ signal. Attenuating the harmonics of the clock frequency will distort the signal and hence the need to characterize the frequency response of transmission media to higher frequencies.

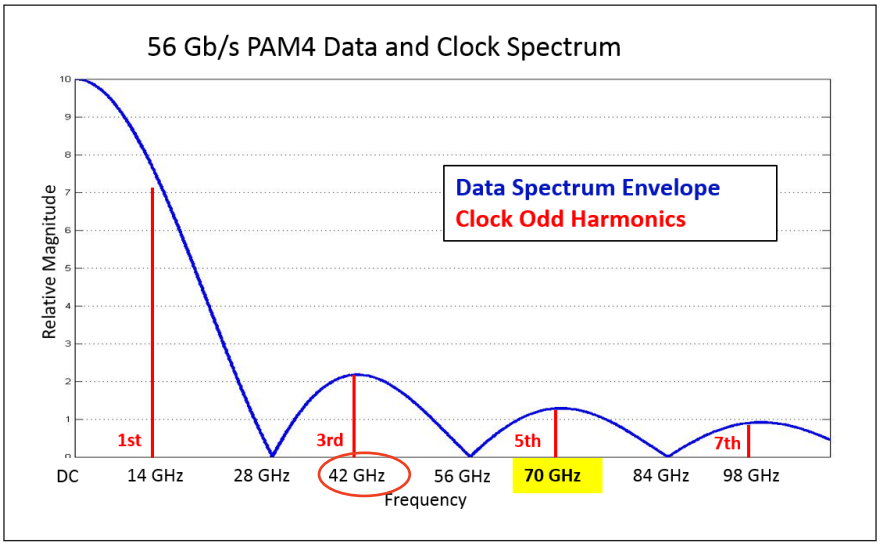


Figure 16. Harmonic Content of 28 Gb/s NRZ Clock Signal.

Today many engineers are working with 56 Gigabit NRZ types of modulations. The fifth harmonic at 56 GB/s NRZ signal is 140 GHz (Figure 17). Anritsu offers the widest single sweep frequency span broadband millimeter wave system to characterize these channels, with a single sweep range of 70 kHz to 145 GHz.

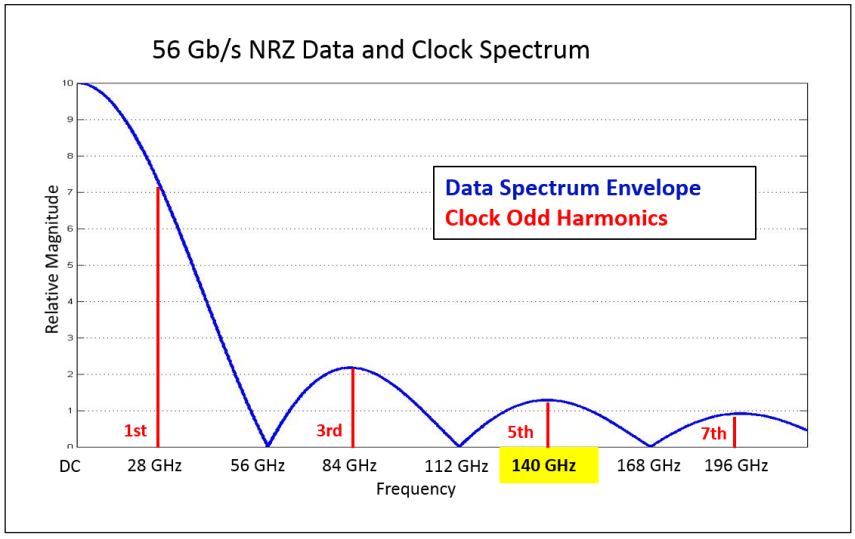


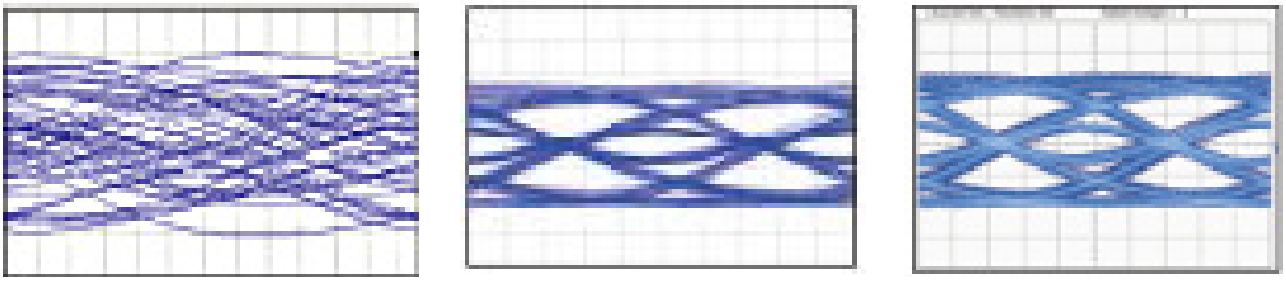
Figure 17. Harmonic Content of 56 Gb/s NRZ Clock Signal.

Minimum Frequency Accuracy

Once the upper frequency need has been addressed, it is time to look at the other end of the spectrum; it is important to remember that accurate measurements to the lowest possible frequency are also very important for signal integrity applications. Often times the accuracy of your models can be improved by measuring down to as close to DC as possible.

For example, consider the case where the measured S-parameter data for a backplane is fed into a software model in order to estimate the impact of that backplane on the eye pattern. Figure 18a shows what the eye pattern estimate will look like when the low frequency data has some error. The error may be from poor dynamic range at lower frequencies or from extrapolation when the data doesn't exist. In this example, it was found that a 0.5 dB error injected at a lower frequency (<10 MHz) on transmission could take an 85% open eye to a fully closed eye. Since mid-band (10 GHz) transmission uncertainty may be near 0.1 dB depending on setup and calibration – and higher at low frequencies – this eye distortion effect cannot be neglected. Figure 18b shows what the resulting eye pattern will look like if the low frequency measurement data is of good quality and extends down to 70 kHz. This prediction correlates very well with the actual eye pattern measured using an oscilloscope as shown in Figure 18c.

Since the non-transitioning parts of the eye-diagram are inherently composed of low frequency behavior, the sensitivity of the calculation to the low frequency S-parameter data makes sense. Because the low frequency insertion losses tend to be small, a large fixed-dB error (which is how VNA uncertainties tend to behave) can be particularly damaging.



(a) 0.5 dB insertion loss error at 10 MHz *(b) Accurate data to 70 kHz* *(c) Actual measured result*

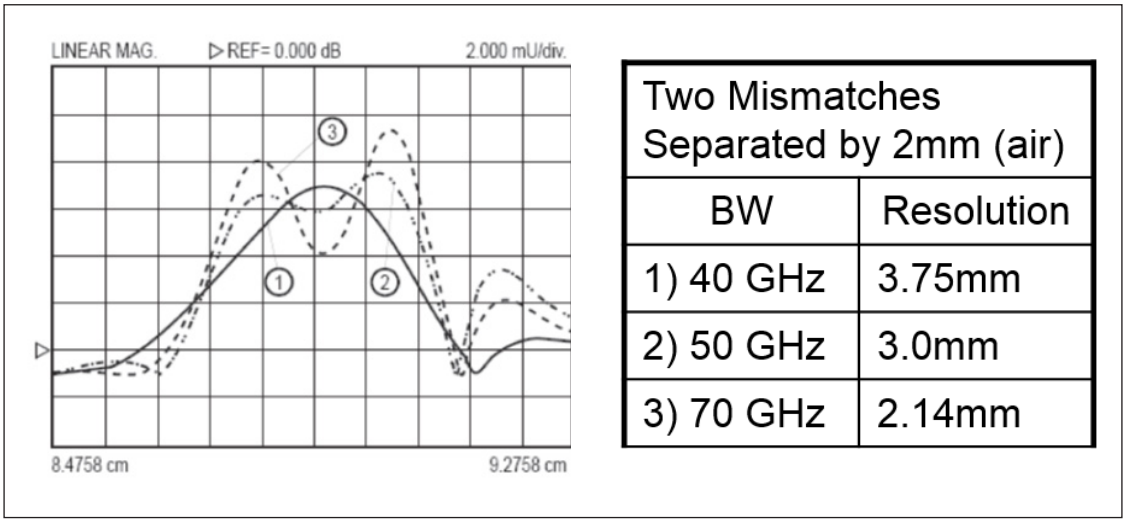
Figure 18. Low frequency errors can result in an open eye appearing to be closed.

Time Domain Considerations

Resolution

Passive components, as well as near-end and far-end points between daughter boards, must be measured in the frequency and time domains to assure that the transmission characteristics at each measurement point meet the standards. Using the best time domain resolution capability improves your ability to locate discontinuities, impedance changes and crosstalk issues.

The time domain performance of a VNA is critical when trying to locate defects. In general, the wider the frequency-sweep, the better is the time, and hence spatial, resolution. Figure 19 shows the differences in time domain resolution for three different frequency spans, 40, 50 and 70 GHz. With only 40 GHz of frequency span, the user is not able to determine there are actually two mismatches present in the channel (as shown by the two peaks in the signal with 70 GHz frequency span). The higher resolution plots can also provide an indication of which mismatch might be the dominant.

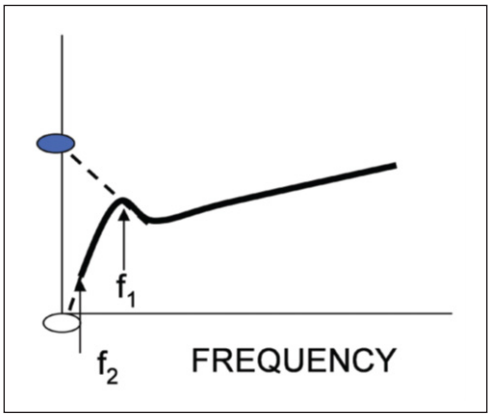


Two Mismatches Separated by 2mm (air)	
BW	Resolution
1) 40 GHz	3.75mm
2) 50 GHz	3.0mm
3) 70 GHz	2.14mm

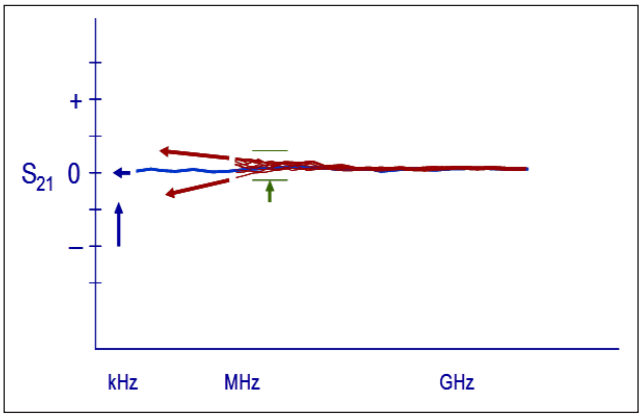
Figure 19. Getting the best time domain resolution requires the most data points, narrowest frequency step size, and widest possible frequency bandwidth.

Low Frequency Accuracy

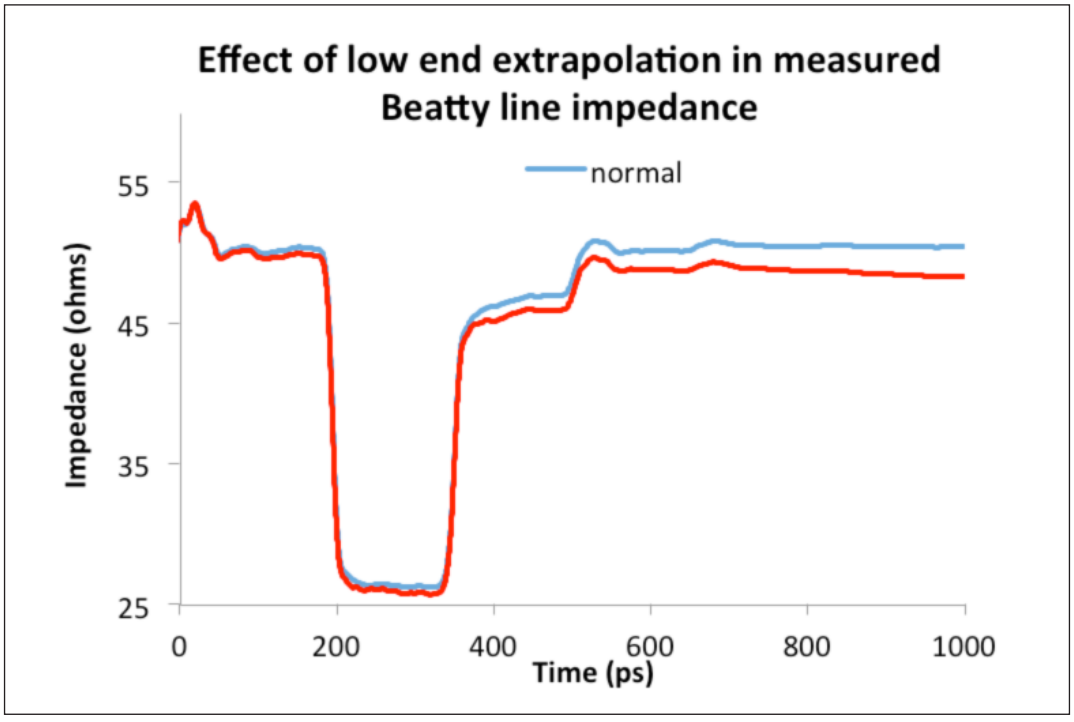
Lack of good low frequency S-parameter data can lead to complications when converting into the time domain for either measurement of impedance changes along a line or for modeling. Longer electrical length DUT's will have more ripple. This structure can make extrapolation of the DC point difficult. In general, the closer you can measure to DC, the better the DC point can be determined (Figure 20a, 20b, and 20c).



(a) DC point extrapolation



(b) Noise and instability

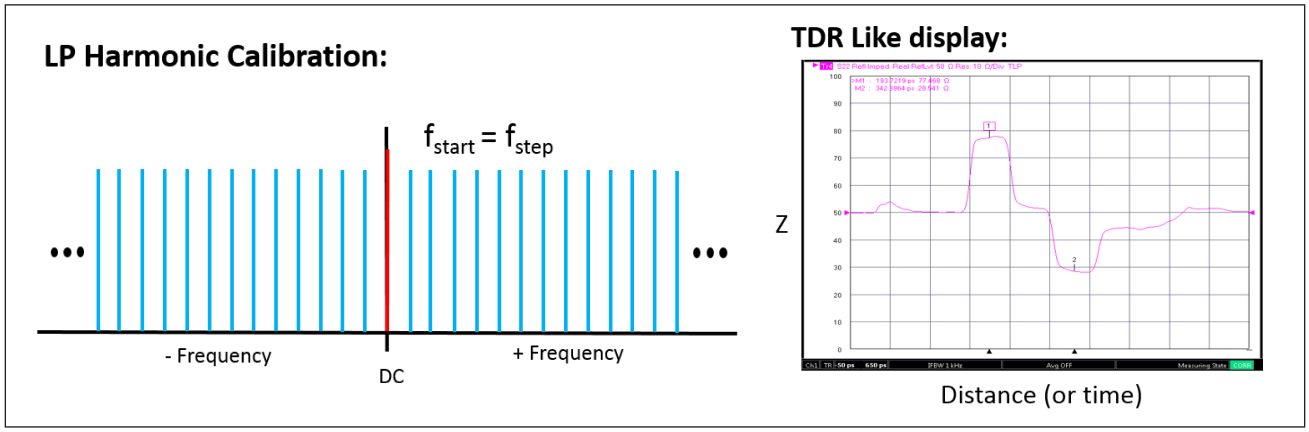


(c) Effect of poor low frequency accuracy

Figure 20. High quality low frequency data enhances the time domain transformation process and quality.

Low-Pass Mode

Resolution is maximized when Low-Pass time domain mode is used. This mode also permits characterization of impedance changes on the backplane. Low-Pass mode requires a quasi-harmonically related set of frequencies that start at the lowest frequency possible (Figure 21a). A DC term is extrapolated that provides a phase reference, so the true nature of a discontinuity can be evaluated. Noise, instability and uncertainty in low frequency S-Parameter data will have an impact on the time domain response and can provide errors in impedance information. Hence, the lower the start frequency with good dynamic range is, the better the extrapolation of the DC term (Figure 21b).



(a) Low pass harmonic calibration *(b) TDR like display*

Figure 21. The VNA Low Pass time domain mode offers the highest resolution.

Alias-Free Range

The VNA time domain transformation is a circular function that repeats at a value called Tmax, which determines the alias-free range. Tmax is related to the frequency step size as shown in this equation:

$$T_{max} = \frac{1}{2f_{step}}$$

The time-domain transformation or step response repeats (aliases) after that value. If your device under test is an electrically long structure, then Tmax needs to be greater than its electrical length. Having very small frequency step sizes can be important when you're looking at long structures like cables or a medium that has a high dielectric constant. As an example, the alias-free range on a PC board with a dielectric constant of 4, if the step size is 40 MHz, results in a 75-inch alias-free range. This means that we are unable to measure anything greater than 75 inches. If the step size is reduced by a factor of 10, to 4 MHz, you get a much longer 750-inch alias-free range.

S-parameter Quality Metrics

The inherent nature of how a VNA operates and its own architecture can create signal integrity measurement issues. In a perfect world, a VNA would take continuous data from DC to infinity. However, with a real VNA there are a finite number of points, determined by the start and stop frequencies and step size. The DC point is an estimate because none of the coupling structures of a VNA can measure all the way down to DC.

There are three S-parameter quality metrics to consider for getting quality measurements: reciprocity, passivity and causality.

Reciprocity

The S-parameters of passive devices are reciprocal, for example S_{12} should be the same as S_{21} in both phase and magnitude. S-parameters measured on VNAs rarely suffer these "reciprocity" problems. One way to estimate the uncertainty of S-parameter measurements is to compare reciprocal S-parameters. If the uncertainty is high, you may need to recalibrate.

Reciprocity is a much greater concern for TDT/TDR-based S-parameters. In addition to their time base jitter and noise problems, the fast rise-time step voltage used by TDT/TDR equipment can cause synchronization problems in the forward and reverse directions.

Poor reciprocity is especially troublesome when measurement results are cascaded in simulation (for system simulation afterwards). The reciprocity errors cause mismatch to propagate incorrectly and the errors can build as the file count increases.

Passivity

Passive devices like interconnects shouldn't have any gain, but gain can appear when the receiver is saturated. It's easy to eliminate passivity problems when you measure S-parameters on a VNA. VNAs are precise instruments that require careful calibration. Passivity problems can be eliminated simply by exercising good lab techniques. Assure that the VNA receivers are not compressed during calibration and measurement, check that all connectors are in good condition and properly torqued and verify that any cables used in the measurement are in good condition and are properly de-embedded.

De-embedding errors are often the source of passivity problems. Small errors can cause channels to appear to have gain. This is most prevalent in fixtures with high insertion loss and low loss DUT's. Anritsu offers a wide range of extraction methods for de-embedding a variety of fixtures and other devices.

After your test setup is calibrated, you can verify good passivity with a high-quality low-loss through, like an airline. If there is the slightest bit of gain across the band you may have some passivity issues. Note that you should not use the through calibration fixture to test passivity since it was part of the calibration.

Causality

The biggest potential weakness in transforming frequency-domain measurements to the time domain comes from the limited bandwidth of measurement equipment.

The Fourier transform from frequency to time requires integration over frequency from 0 to infinity, that is, from DC to very high frequency. For example, since the frequency content of a real PAM4 signal rarely exceeds the fifth harmonic, 5/2 fbaud (where fbaud is the baud rate and ½ fbaud is the fundamental), we can approximate the upper integrand, $\infty \approx$ 5/2 fbaud or larger. The trouble comes at the bottom end. Since we can't generate a DC sine wave, we can't measure the S-parameters all the way down to DC: the DC limit of the S-parameters must be extrapolated. The best that we can do is use equipment that gets as close to DC as possible.

[Note: Bits per second is straightforward. If 1000 bits are being sent at 1000 bps, it will take exactly one second to transmit them. Baud is symbols per second. If these symbols — the indivisible elements of your data encoding — are not bits, the baud rate will be lower than the bit rate by the factor of bits per symbol. That is, if there are 4 bits per symbol, the baud rate will be ¼ that of the bit rate.]

High start frequencies cause causality problems that give the appearance of effects preceding their causes, like an output that occurs prior to its input and convergence problems in the time domain (Figure 22). Anritsu VNAs reduce the causality and convergence risks by reaching down to the lowest VNA frequency in the industry.

Time domain S11 measurements in log mag displays

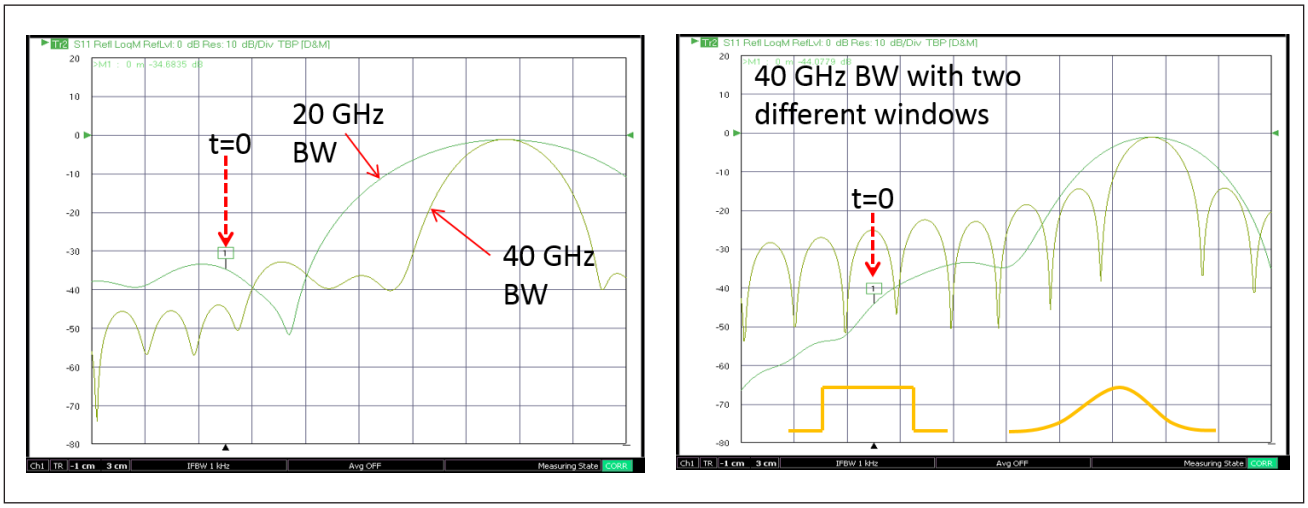


Figure 22. Basic causality is always impacted by available finite bandwidth. VNAs offer multiple time domain windowing functions (right), which can also have a major effect on the measured result. Note the signal levels for t<0.

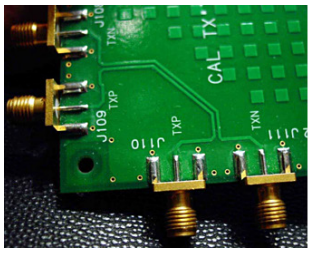
Accurately Remove Fixturing Effects

Higher data rates can create challenges for traditional de-embedding techniques. As frequencies approach 70 GHz or even 110 GHz, errors related to fixturing can be greater than those of the "device under test" or DUT. Fixtures and connectors to DUTs come in many forms. Poor de-embedding can lead to both passivity and causality errors. In addition, high fixture loss may affect the accuracy and repeatability of de-embedding. Achieving accurate measurements at these higher frequencies offers the advantage of improved ability to locate discontinuities, impedance changes, and crosstalk issues.

There are many situations where it may not be possible to connect directly to the DUT. Say we're interested in how a signal looks at the test point in Figure 23. If we measure the S-parameters of everything between the test equipment and the test point, we can "de-embed" the effect of the test fixture and reveal how the signal appears at the test point.

Figure 23. The test fixture must be de-embedded from measurements so that we can evaluate the signal at the test point.

Sometimes the opposite is required: it may be useful to take a device and assess its performance when it is surrounded by other networks. Embedding techniques allow you to insert the effects of network elements by using the S-Parameters of one or more connectors or fixtures on one or both test ports (Figure 24).



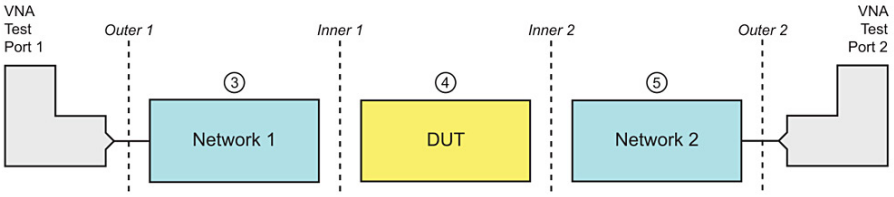


Figure 24. Embedding techniques allow you to insert the effects of network elements by using the S-Parameters of one or more connectors or fixtures on one or both test ports.

Anritsu offers a wide range of techniques available that can handle different situations (Table 1). By matching the calibration and de-embedding method to your specific DUT and fixture structures you will improve the accuracy and repeatability of your measurements.

Method	Standards Complexity	Fundamental Accuracy	Sensitivity to Standards	Media Preferences
Type A (Adapter Removal)	High	High	High (refl.)	Need good reflect and thru stds
Type B (Bauer-Penfield)	Medium	High	High (refl.)	Only need reflect standards, not great for coupled lines
Type C (Inner-Outer)	High	High	Medium (refl.)	More redundant than A so less sensitive but need good stds still
Type D (2-Port Inner-Outer)	Medium	Low for low-loss or mismatched fixtures	Medium (line def'n.)	Only need decent lines; match relegated to lower dependence; can handle coupled lines
Type E (4-Port Inner-Outer)	High	High	Medium (refl.)	Somewhat redundant (like C) but need decent standards. Best for uncoupled multiport fixtures
Type F (4-Port Uncoupled)	Medium	Low for low-loss or mismatched fixtures	Medium (line def'n.)	Only need decent lines; match relegated to lower dependence; can handle coupled lines
Type G (4-Port Coupled)	Medium	Low for low-loss or mismatched fixtures	Medium (line def'n.)	Only need decent lines; match relegated to lower dependence; can handle coupled lines well
Type H (Time Domain-Based)	Low	Can be low for lossy or complex fixtures (many structures per wave length)	Low	Best for electrically large structures

Table 1. De-embedding Methods

Superposition vs. True Mode Stimulus

Signal Integrity applications commonly utilize balanced/differential transmission lines which are typically characterized using VNAs. There are two approaches to performing these measurements and the selection of the best method depends on what you need to measure.

The "Superposition technique" relies on the inherent linear nature of a transmission line and mathematically derives the differential and common-mode transmission line characteristics through superposition while stimulating just one side of the differential transmission line at a time. The "True Balanced/ Differential technique" uses two sources to create actual differential and common-mode stimuli, hence the shortened name "true mode stimulus" or TMS (Figure 25).

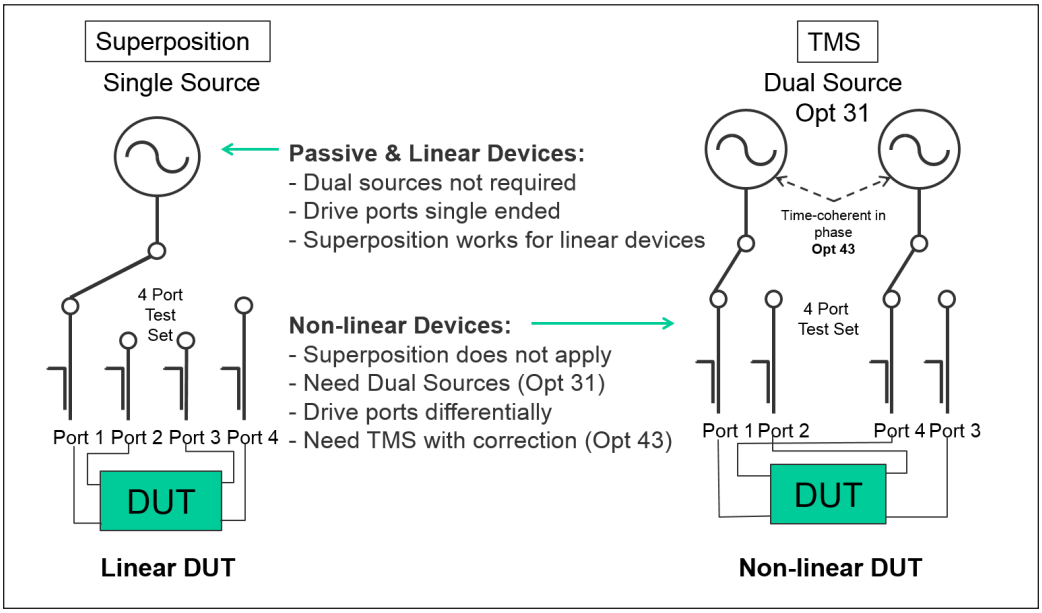


Figure 25. Superposition vs. True Mode Stimulus

Most signal integrity measurements are of passive components such as transmission lines, PCBs, cables and connectors. For passive devices, the superposition technique is widely accepted to generate the required differential and common-mode responses from a differential device. Even active devices, if kept in their linear region, can be accurately tested using the superposition technique (Figure 26). For active devices that are driven into compression or saturation, the true mode stimulus technique is required.

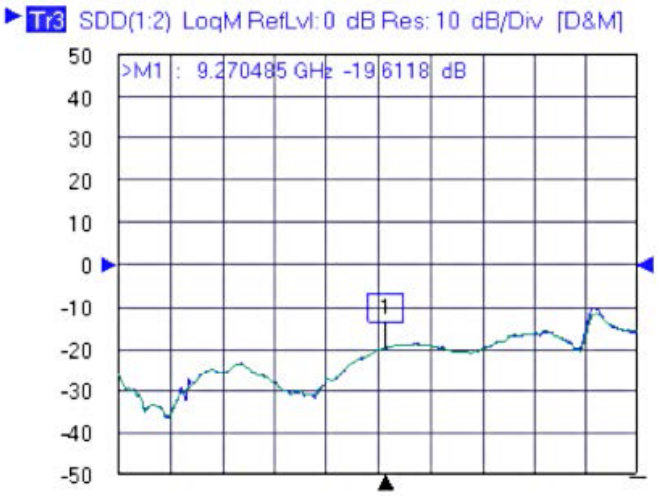


Figure 26. Comparing single-ended and TMS mode measurements of linear differential amplifier reveals minimal differences.

Determining which measurement technique is best for you is fairly straightforward. If you are measuring passive devices or active devices that stay in their linear range, then the superposition technique offers the simplest, most stable and lowest cost solution. The added cost, calibration complexity and stability concerns of the true mode stimulus solution are only worth it if you are testing active devices in their non-linear range.

Summary

Higher data rates require accurate measurements to provide the confidence needed to achieve the desired performance. Measurement tools must help shorten design times and ensure stable signal integrity in mass production. VNAs play a key role in helping both the RF and signal integrity engineers meet the performance challenges of increasing data rates. This paper provided a review of signal integrity-based VNA measurements for digital engineers and correlated VNA measurements to key signal integrity parameters for RF engineers. For those needing to increase their current measurement performance, Anritsu offers a wide range of test equipment that is designed to meet both your budget and performance needs for either R&D or manufacturing.

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